

Replacement Sheet

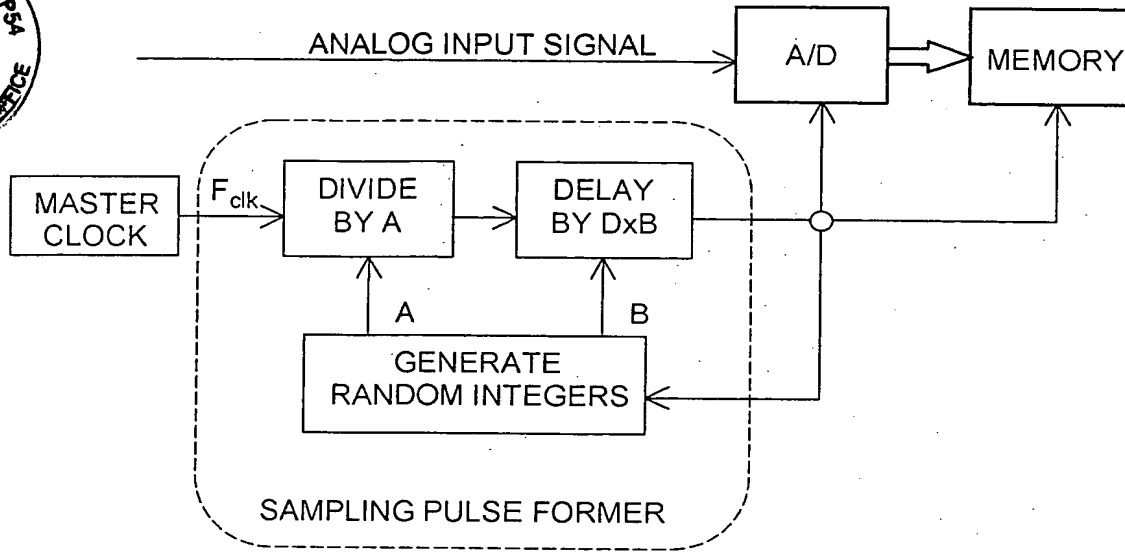


FIG.1. A schematic block diagram of the present invention

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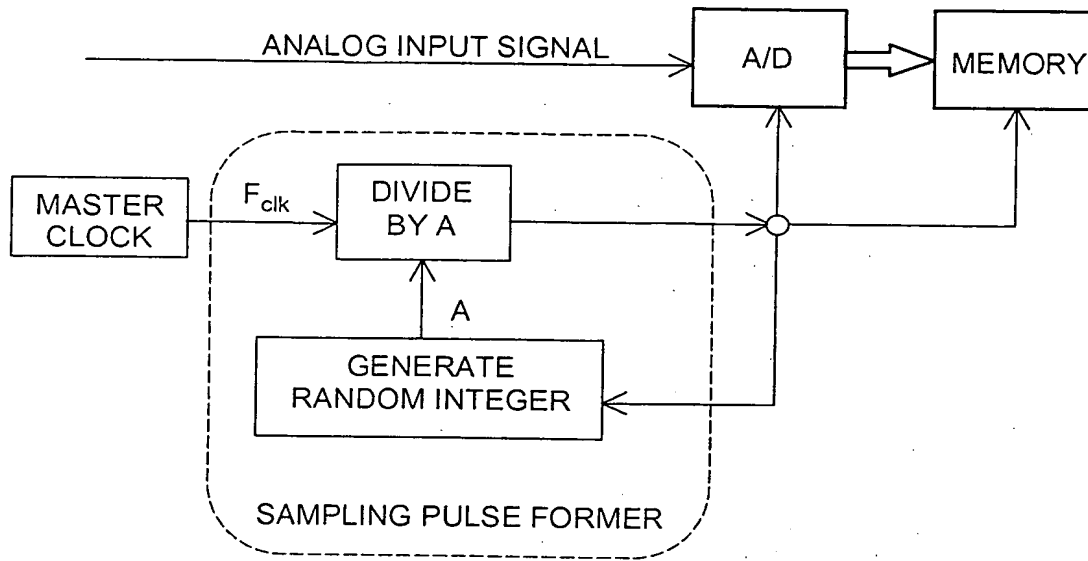


FIG. 2. A schematic block diagram of a priori art circuit

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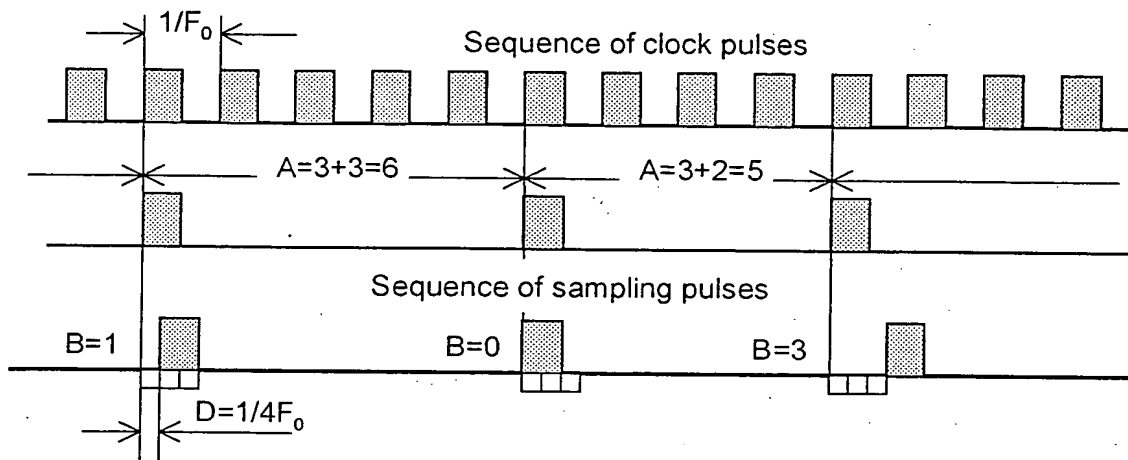


FIG.3. A time diagram showing the manner in which the sampling pulses are formed

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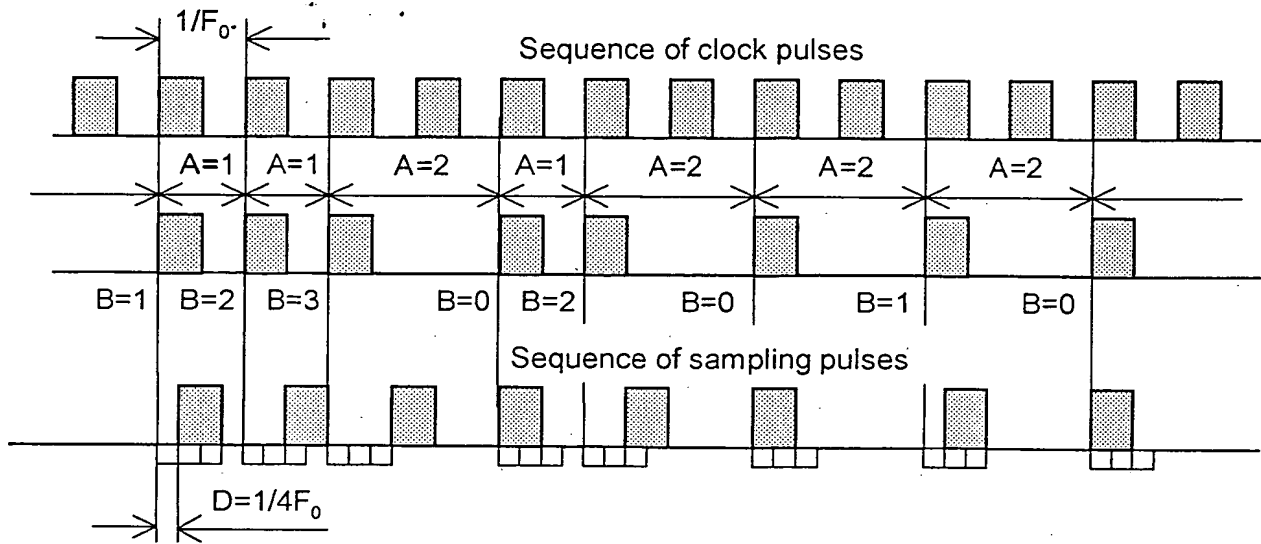


FIG.4. A time diagram showing the manner in which the sapling pulse sequence is adapted to the highest rate operation